Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-2 (Canceled)

Claim 3 (Previously Presented): The method according to claim 21, wherein the predetermined temperature is a temperature of from 200°C to 400°C.

Claim 4 (Previously Presented): The method according to claim 21, wherein the metallic layer is formed on the silicon region by a long throw sputtering method or a collimate sputtering method.

Claim 5 (Previously Presented): The method according to claim 21, wherein the metallic layer is comprised of titanium, cobalt or nickel.

Claim 6 (Previously Presented): The method according to claim 21, wherein a depth of the silicon region is larger than the first thickness of the metallic layer.

Claim 7 (Previously Presented): The method according to claim 21, wherein the

protective layer is comprised of titanium-nitride or tungsten.

Claim 8 (Previously Presented): The method according to claim 21, wherein the first thickness of the metallic layer is equal to or less than 15nm.

Claim 9 (Previously Presented): The method according to claim 21, wherein the second thickness of the protective layer is equal to or more than 30nm.

Claim 10 (Previously Presented): The method according to claim 21, wherein a source region and a drain region of an MOS transistor are formed in the silicon region, wherein the metallic silicide layer is formed in the source and drain regions.

Claims 11-20 (Canceled)

Claim 21 (Currently Amended): A method for fabricating a semiconductor device, comprising:

preparing a substrate having a silicon region;

heating the substrate at a predetermined temperature;

forming a metallic layer on the silicon region of the heated substrate by a straight sputtering method so as to sputter straightly to the silicon region, wherein the metallic layer has a first thickness;

forming a protective layer on the metallic layer, wherein the protective layer protects the metallic layer from a surrounding atmosphere and wherein the protective layer has a second thickness greater than the first thickness; [[and]]

forming a metallic silicide layer in an interface between the silicon region and the metallic layer under the protective layer by a first heat treatment, so that the metallic silicide layer has a high resistance crystalline structure;

removing the protective layer; and

subjecting the metallic silicide layer to a second heat treatment after said removing the protective layer, so that the metallic silicide layer has a low resistance crystalline structure ~~after said forming a protective layer, wherein the metallic silicide layer is comprised of metal from the metallic layer and silicon from the silicon region~~.

Claim 22 (Currently Amended): The method according to claim 10, wherein the MOS transistor also includes a polysilicon gate, said forming a metallic layer comprises forming the metallic layer on the gate, and

~~Wherein~~ wherein the metallic silicide layer is formed in an interface between the polysilicon gate and the metallic layer.

Claim 23 (New): A method of manufacturing a semiconductor device, comprising:

preparing a substrate having a silicon region thereon;

heating the substrate at a predetermined temperature;

forming a metallic layer on the silicon region of the heated substrate by a straight sputtering method;

forming a protective layer on the metallic layer;

forming a first metallic silicide layer on the silicon region under the protective layer by a first heat treatment, the first metallic silicide layer having a high resistance crystalline structure;

removing the protective layer; and

subjecting the first metallic silicide layer to a second heat treatment after said removing the protective layer, so as to change the first metallic silicide layer into a second metallic silicide layer having a low resistance crystalline structure.

Claim 24 (New): The method of manufacturing a semiconductor device according to claim 23, wherein the metallic layer is comprised of titanium, cobalt or nickel.

Claim 25 (New): The method of manufacturing a semiconductor device according to claim 23, wherein the predetermined temperature is a temperature of from about 200°C to about 400°C.

Claim 26 (New): The method of manufacturing a semiconductor device according to claim 24, wherein the metallic layer is comprised of titanium.

Claim 27 (New): The method of manufacturing a semiconductor device according to claim 26, wherein the first metallic silicide layer is a Ti_2Si layer and the second metallic silicide layer is a $TiSi_2$ layer.

Claim 28 (New): The method of manufacturing a semiconductor device according to claim 26, wherein the metallic layer has an orientation of a (200) surface.

Claim 29 (New): The method of manufacturing a semiconductor device according to claim 23, wherein a temperature of the first heat treatment is lower than a temperature of the second heat treatment.

Claim 30 (New): A method of manufacturing a semiconductor device, comprising:

providing a substrate having a silicon region thereon;

heating the substrate at a predetermined temperature;

forming a metallic layer on the silicon region of the heated substrate by a straight sputtering method;

forming a protective layer on the metallic layer;

forming a high resistance metallic silicide layer on the silicon region under the protective layer by a first heat treatment, the high resistance metallic silicide layer having a first crystalline structure;

removing the protective layer; and

subjecting the high resistance metallic silicide layer to a second heat treatment after said removing the protective layer, so as to change the high resistance metallic silicide layer into a low resistance metallic silicide layer having a second crystalline structure.

Claim 31 (New): The method of manufacturing a semiconductor device according to claim 30, wherein the predetermined temperature is equal to or higher than about 200°C and is lower than about 400°C.

Claim 32 (New): The method of manufacturing a semiconductor device according to claim 30, wherein the metallic layer is comprised of titanium.

Claim 33 (New): The method of manufacturing a semiconductor device according to claim 32, wherein the first metallic silicide layer is a Ti_2Si layer and the second metallic silicide layer is a $TiSi_2$ layer.

Claim 34 (New): The method of manufacturing a semiconductor device according to claim 32, wherein the metallic layer has an orientation of a (200) surface.

Claim 35 (New): The method of manufacturing a semiconductor device according to claim 32, wherein a temperature of the first heat treatment is lower than that of the

second heat treatment.